



COMSATS UNIVERSITY ISLAMABAD (CUI)
DEPARTMENT OF COMPUTER SCIENCE
TERMINAL EXAMINATION FALL - 2022
BS (CS) - 4th SEMESTER

Course: CSC-325 Computer Organization & Assembly Language
Maximum Marks: 50

Dated: January 25, 2023

Instructor: Taimur Shahzad
Time Allowed: 180 Minutes

- All questions are self-explanatory and require no further explanations during exam time.
- Make sure that you have signed the attendance sheet before leaving the examination room.
- Return the question paper along with the answer sheet.
- Attempt all questions.

(CLO - 1: Articulate the components of a computer along with its architecture)

QUESTION NO.01:

- Differentiate between pipelined and non-pipelined processors. What is the advantage of pipeline over non pipelined execution? [05 Marks]
- Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate-? [05 Marks]

$$\frac{80}{4} = 20$$

$$20 \times 4 = 80$$

$$80 + 10 = 90$$

$$280 \times 1000 = 280000$$

 - Non-pipeline execution time.
 - Speed up ratio.
 - Pipeline time for 1000 tasks.
 - Sequential time for 1000 tasks.
 - Throughput.

(CLO - 2: Review memory systems and its hierarchy along with IO methods)

QUESTION NO.02:

- Demonstrate the memory hierarchy of computer and define the concept of locality of reference in memory. [02 Marks]
- Consider a system having 32K bytes of main memory and 512 bytes of cache memory. The block size for both the memories is equal to 16 bytes. How many bits will be kept for offset, set number and tag bits for 8-way set associative cache? [05 Marks]
- Assume that a processor has a direct mapped cache, the physical address is 20 bits long, the tag is 12 bits, and each block holds 32 bytes of data. How many lines are in this cache? [05 Marks]

Let's say CPU sends requests for the following sequence of addresses:

0011 0101 0110 1101 1010,	0000 0011 1101 0111 0001,	0011 0101 0110 1101 0000,
1000 0000 1101 0111 0111,	1111 0010 0000 0000 1000,	1111 0010 0000 0001 0110,
1010 1010 1010 1100 0001,	1000 0000 1101 0111 0111	

For each of the requests, state if it would result in a cache hit or a cache miss. Also show the final state of tag registers once all the requests have been entertained. Assume that the whole cache is free at the start.

[10 Marks: 2+3+5]