COMSATS University Islamabad (CUI), Islamabad

Department of Electrical & Computer Engineering

CPE241 Digital Logic Design

Terminal Exam Fall 2022

Instructor: Dr. Babar Mansoor
Max Marks: 50

Class: BCE2R
Time Allowed: 3 Hours

Q(1) (6 Marks), [CLO2,C3]

(a) **(3 Marks)** Implement $F = xy + x'y' + y'z$ using NAND gates only.

(b) **(3 Marks)** Express $F(A, B, C, D) = \prod(3, 5, 7)$ in sum-of-minterms form.

Q(2) (4 Marks), [CLO3,C4]

Simplify the following Boolean function F, together with the dont-care conditions d , and then express the simplified function in sum-of-minterms form. Also draw the logic circuit corresponding to the obtained sum-of-minterms expression.

$$F(A, B, C, D) = \sum m(0, 6, 8, 13, 14) + \sum d(2, 4, 10)$$

Q(3) (10 Marks), [CLO4,C5]

(a) **(5 Marks)** Design a 3-bit magnitude comparator circuit.

(b) **(5 Marks)** Design a 4-to-16-line decoder using 2-to-4-line decoders with enable input.

Q(4) (10 Marks) [CLO3,C4]

Analyze the circuit shown in Figure 1 by obtaining the next-state and output equations, state transition table and state diagram. Also complete the timing diagram shown in Figure 2.

Q(5) (10 Marks), [CLO4,C5]

Design a synchronous sequential circuit for the state diagram shown in Figure 3 using positive edge triggered JK flip-flops.

Q(6) (10 Marks), [CLO4,C5]

(a) **(5 Marks)** Design a 3-bit ripple down counter using T flip-flop. Also draw the corresponding time diagram for the obtained circuit.

(b) **(5 Marks)** Design a 4-bit left-shift register using negative edge triggered D flip-flops and four 4-to1 multiplexers.The shift register has two external input signals Sh and Ld such that register should shif left if $Sh = 1$, load if $Sh = 0$ and $Ld = 1$ and hold its state if $Sh = Ld = 0$. Also write the next-state equations for the flip-flops.

JA = BX', KA = X, JB = AX, KB = X

Z = X ⊕ B

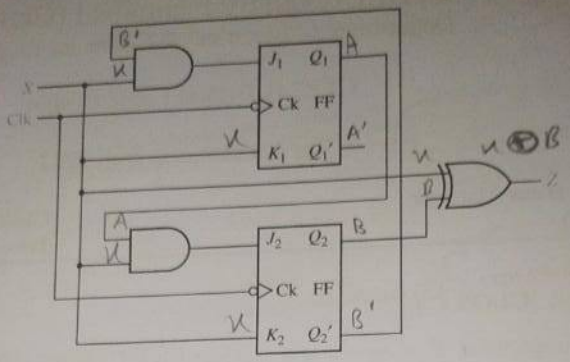

Figure 1: Circuit for Q(4)

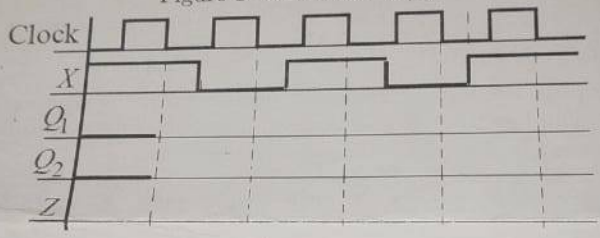

Figure 2: Timing diagram for Q(4)

JA = XB

KA = B ⊕ X

JB = X

KB = A

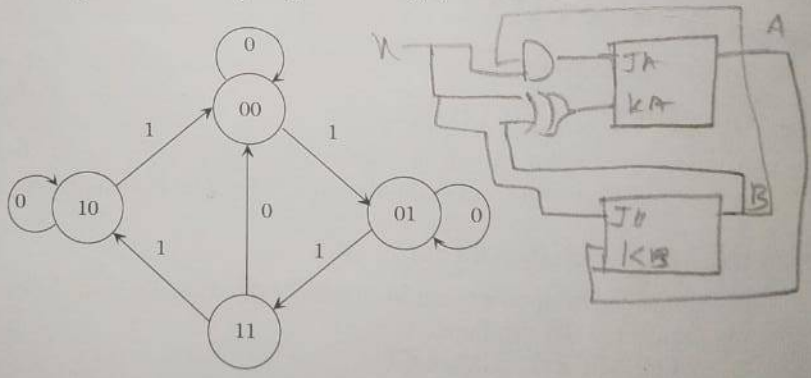

Figure 3: State diagram for Q(5)

The End

COMSATS UNIVERSITY ISLAMABAD (CUI)
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Terminal Exam – FA22

EEE241 Digital Logic Design

Marks: 50 | **Time: 3 Hours**
Date: 20th January 2023 | **Instructor: Dr. M. Rizwan Azam**
Class: BDS 2A

Question No. 1 **(5+5 marks)**

a. Simplify the following Boolean function by first finding the essential prime implicants

$$F(A,B,C,D) = \sum(1,3,4,5,10,11,12,13,14,15)$$

b. Design 3-input majority circuit by finding the circuit's truth table, Boolean equation, and logic diagram. Note that a majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise.

Question No.2 **(10 marks)**

Design a combinational circuit that generates the 9's complement of a BCD Code.

Question No. 3 **(10 marks)**

Design a combinational circuit that multiplies a binary number "B" represented by four bits by a binary number "A" represented by three bits.

Question No. 4 **(10 marks)**

A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are

$$J_A = Bx + B'y', \quad K_A = B'xy' \quad J_B = A'x,$$
$$K_B = A + xy', \quad z = Axy + Bx'y'$$

a) Draw the logic diagram of the circuit.
b) Tabulate the state table.
c) Derive the state equations for A and B.

Question No. 5 **(10 marks)**

Design a circuit that detects a sequence of three or more consecutive 1's in a string of bits coming through an input line. Present state diagram, state table, state equations and logic diagram.

********** GOOD LUCK **********