

Q No.4)

(5+5=10 marks)

- Design a 16-to-1 multiplexer using 2-to-1 multiplexers. Use as many MUX of 2-to-1 you need.
- Design a Full adder circuit by using multiple 2 to 4 line decoders.

Q No.5)

(3+4=7 marks)

- Design a logic circuit with minimum numbers of gates represented by the truth table given below in sum of Product form and product of sum form.

x	y	z	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

- For the Boolean Function $F(ABCD) = ABC' + BC'D' + CD + A'B$, Implement the simplified expression with NOR gate only.

Q No.6)

(7 marks)

What are shift registers? Draw the block diagram to explain its application of serial to parallel data conversion. Explain the working with an appropriate timing diagram.

***** GOOD LUCK *****